memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.--

--67. (New) A method for extending the life of Flash EEprom memory in a Flash EEprom system, comprising the steps of:

temporarily storing data files from a host system intended for the Flash EEprom memory in a cache memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

storing the identity of data files and the time each data file was last written into said cache memory in a tag memory;

in response to a write request from the host system, writing a data file into the Flash EEprom memory when the data file is not identified in the tag memory, or into the cache memory when the data file is identified in the tag memory; and

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by reference to the tag memory, moving data file having the longest time since last written first from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.--

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Remarks:

Claims 1-29 and 56-62 directed to a non-elected invention are being canceled in this application.

The title of the invention is being amended to be more clearly indicative of the invention to which the claims are directed.

The Examiner has objected to the consistency of the depiction of the controller shown in Figures 1, 2, 3A, 3B, 6 and 7.

The confusion may have arisen from the inadvertent errors in the brief description of Figure 3A on page 5, lines 11-12. It

consistent with the figures as well as descriptions on page 9, lines 30-33.

Applicants propose to amend Figure 3A by using a bar under numeral 220 to indicate the scope of numeral 220. It will then be clear from the figure as well as from context that it refers only to the block circuit diagram on a Flash EEprom chip and does not include the sectors 211, 213.

As for Figures 6 and 7, they are essentially the same as block 29 shown in Figure 1A. Block 29 comprises a controller 31 in communication with a memory array 33. Both Figure 6 and 7 comprise controller 31 and memory 33 demarcated by a partition. Thus, apart from the memory 33, all are functional blocks of the controller 31.

The Examiner has rejected claims 30-55 under U.S.C. 112, 2nd paragraph, "as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention."

Claims 34, 40, 48, and 54 are being canceled.

Claims 32, 38, 44, 52 are being amended to correct typographical errors so that they are now correctly dependent on their preceding claims as originally intended.

All claims in the application, 30-33, 35-39, 41-47, 49-53 and 55, are being amended to more clearly recite the interrelationship among the claimed elements and to define the invention.

Regarding the Examiner's comments 6(a) and 6(b), all independent claims 30, 36, 42, 46 and 51 are being amended to relate the invention to "an improved Flash EEprom system with reduced write-related stress." It is now clearer that claimed elements, such as "a Flash EEprom memory", "cache memory" "controller" and "timing means" are all part of the improved Flash EEprom system. The interrelationship among claimed elements is apparent from the recitation of the controller and its operations

Regarding the Examiner's comment 6(c), all independent claims 30, 36, 42, 46 and 51 are also being amended to implicitly express the "write request" as coming from "the host system".

Regarding the Examiner's comment 6(d), claims 31, 37, 43 and 51 are being amended from the language "means responsive to an impending power loss" to --said controller responsive to a power loss in the host system--.

Regarding the Examiner's comment 6(e), it is clear that the Flash EEprom memory and the controller are different claimed elements of the improved Flash EEprom system (see response to comment 6(a) and 6(b) above). In any case, claims 31, 37, 43 and 51 are being canceled in this application.

It is believed that the above amendments to the claims overcome the 35 U.S.C Section 112, second paragraph objections by the Examiner.

New claims 63-67 directed to methods for extending the life of Flash EEprom memory in a Flash EEprom system are being added in this application. By virtue of the remarks regarding the independent claims, they are also believed allowable.

The Examiner also rejected claims 30-55 under 35 U.S.C. Section 103 as being unpatentable under Furiya et al. in view of Terada et al.

Conventional EEprom and Flash EEprom have a limited lifetime due to the endurance-related stress the device suffers each time it goes through an erase/program cycle. The endurance of a Flash EEprom device is its ability to withstand a given number of program/erase cycles. The physical phenomenon limiting the endurance of conventional EEprom and Flash EEprom devices is trapping of electrons in the active dielectric films of the device. During programming (write), electrons are injected from the substrate to the floating gate through a dielectric interface. Similarly, during erasing, electrons are extracted from the

interface. The trapped electrons oppose the applied electric field in subsequent program/erase cycles thereby causing the programmed threshold voltage to shift to a lower value and the erased threshold voltage to shift to a higher value. This can be seen in a gradual closure in the threshold voltage "window" between the "0" and "1" states. Beyond approximately 1×10^4 program/erase cycles the window closure can become sufficiently severe to cause the reading circuitry to malfunction. If cycling is continued, the device eventually experiences catastrophic failure due to a ruptured dielectric. This typically occurs at between 1×10^6 and 1×10^7 cycles, and is known as the intrinsic breakdown of the device. Thus, with use, defects tend to build up in the memory array and typically the devices are rendered unreliable after 10^3 to 10^4 write/erase cycles.

Another problem associated with write operations in EEprom devices is the tendency for write in one portion of the memory to disturb the memory state of cells in other portion of the memory. The disturbance is cumulative, and over time may cause the disturbed cells to render errors.

Since, data can be programmed only into an erased EEprom memory cell, increasing write or program operations entails increasing erase operations, both of these are stressful to the EEprom devices.

Thus, generally it is desirable to minimize the number of write to EEprom devices. Traditionally, EEprom and Flash EEprom are used in applications where semi-permanent storage of data or codes is required but with a limited need for reprogramming.

Applicants' claimed invention relates to an improve Flash EEprom system wherein the no of write operation, is reduced by the use of a write cache. In this way, the useful lifespan of the device may be extended, thereby making it more amenable to be used in applications where a magnetic disk drive is traditionally

Furiya discloses read and write caches for the conventional purpose of improving access of magnetic disks. Improvement is realized because the access speed of the solid-state memory used for the cache memory is typically ten times faster than that of the magnetic disks. Furiya does not teach nor suggest the use of a write cache to reduce stress to an electrically erasable and programmable read-only memory (EEprom).

Terada discloses an improved read circuit for an EEprom. There is no teaching of write cache nor the use thereof to reduce stress in an EEPROM.

There is therefore no teaching or suggestion by Furiya or Terada, individually or in combination, of an improved Flash EEprom system with reduced write-related stress by employing a write cache. Merely substituting Furiya's magnetic disks with Terada's EEprom does not teach the use of a write cache to reduce write stress in Flash EEprom. In any case, it is not obvious to substitute Furiya's magnetic disks with Terada's EEprom. As explained above, traditional EEprom and Flash EEprom are used in applications where semi-permanent storage of data or codes is required but with a limited need for reprogramming. Whereas, in the environment contemplated by a magnetic disk, the much increased number of write/erase cycling would be considered beyond the capacity of the EEprom devices.

Claims 30-33, 35-39, 41-47, 49-53, 55 and 63-67 are now pending. In view of the Amendments and explanations given, reconsideration of the rejections is requested.

It is believed that this application is now in condition for allowance and an early indication thereof is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 13-1030.

Respectfully submitted,

Philip Yau, Reg. No. 32,892

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MAJESTIC, PARSONS, SIEBERT & HSUE
Four Embarcadero Center, Suite 1450
San Francisco, CA 94111-4121
Telephone: (415) 362-5556
Facsimile: (415) 362-5418

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